Laboratory 13: JFETS, MOSFETS, CMOS and Applications

Concept

(Simpson)
The field affect transistor (FET) is a special type of transistor which offers a number of advantages in some applications over the bipolar transistors used in previous labs. FET advantages include considerably higher input impedance, lower noise, and higher resistance to nuclear radiation damage. The high input impedance is important in applications where the signal source driving the FET has high output impedance or where very small currents must be amplified. If the FET input impedance is much higher that the source output impedance, then little signal is lost due to impedance mismatch (the source is not appreciably "loaded"). In general, however, the gain available from an FET is less than from a carefully selected bipolar transistor. Because a FET carries current only by the flow of majority carriers, it is sometimes termed a "unipolar" transistor, although the term FET is more common. An ordinary transistor is often termed a "bipolar" transistor to distinguish it from a FET, because it carries current by the flow of both majority and minority carriers. In a pnp bipolar transistor, for example, the holes are majority carriers in the emitter and the collector, but are minority carriers in the base.

We have a few different terms to define:

- Drain, source, and gate voltages V_D, V_S, V_G
- Drain-source current, voltage I_{DS}, V_{DS}
- Gate-source current, voltage I_{GS}, V_{GS}
- Pinch-off gate-source potential V_{po} or $V_{GS}(\text{off})$

Helpful hints and warnings

When measuring different voltages across the transistor, remember that the difference amplifier is only required when you wish to measure a changing signal. For DC voltages, your DMM works great and is easy to set up. Use your simplest tools first to gather the basic information like the pinch off gate-source voltage V_{po}. This requires that you measure the potential difference across the gate-source junction at some DC input voltage, and your DMM will work just fine for that. However, to measure a current through R_D and a potential difference across the drain-source junction simultaneously, you will need two difference amplifiers.

Also, make sure you are always reverse biasing the gate to avoid any forward bias gate-source currents. This can be verified by analyzing the doped semiconductor layers of the transistor, and ensuring that the depletion zone will be increased by the gate potential that you are going to use.

Experimental Instructions

13.1 Common Source Junction Field Effect Transistor

Background:
As the magnitude of the gate voltage is increased (make sure you have the sign correct for the type of JFET being used), the current decreases. At some V_{GS}, the drain-source current I_{DS} will reach a minimum (very close to zero because the reverse bias gate-source current I_{GS} is very small compared to I_{DS}. Remember that there are multiple ways to conduct the following measurements, some ways will require one difference amplifier, but others will require two.

Instructions:

1. Build a difference amplifier with a gain of ≈1. Measure the gain of the difference amplifier from 10^2 to 10^7 Hz.
2. Build the simple JFET circuit. Find the pinch-off gate-source potential V_{po} by varying the gate potential (increasing from 0) until the channel current I_{DS} approaches 0.

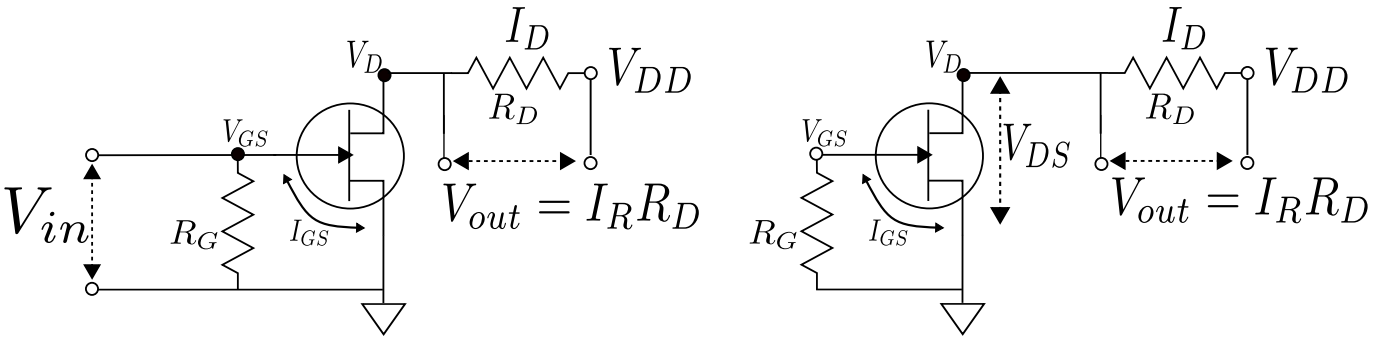

Figure 13.1: (left) Simple PNP (n-channel) JFET circuit, and (right) emphasis of our measurements.

3. Record several $I_{DS}(V_{DS})$ curves at various DC gate voltages $V_{po} < V_{GS} < 0$ when V_{DD} is a ramp wave at 1 kHz.
4. Record $I_{DS}(V_{DS})$ at one or more DC gate voltages $V_{po} < V_{GS} < 0$ when V_{DD} is a sine wave at 1 kHz and 20 MHz.

Questions to answer:

1. What is the gain of each of your difference amplifiers?
2. What is the pinch-off gate-source potential V_{po}?
3. Graph and explain the $I_{DS}(V_{DS})$ curves from the ramp wave.
4. Graph and explain the $I_{DS}(V_{DS})$ curves from the sine waves. Discuss the frequency dependence compared to the BJT.

13.2 n-channel Enhancement Mode MOSFET

Background:

As the gate voltage is increased the drain-source current I_{DS} increases. There are multiple ways to take the following measurements–find the way to measure the fewest voltages and still get all the information you need.

Instructions:

1. Using the BS170 n-channel enhancement mode transistor, build the simple JFET circuit. Use your differential amplifier to measure the drain current I_D.

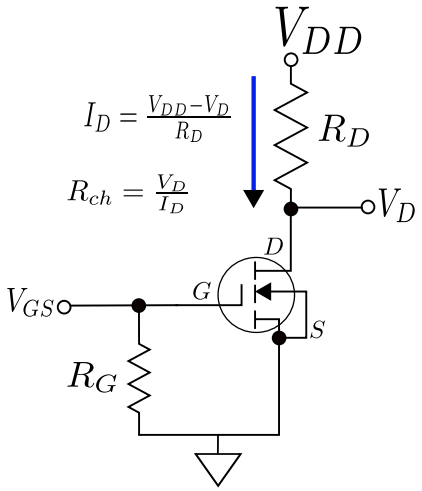

Figure 13.2: A simple n-channel enhancement mode MOSFET circuit.

2. Measure the channel resistance R_{ch} by measuring the voltage over the drain resistor $(V_{DD} - V_D)$ as a function of the gate voltage V_{GS}. Use a sine wave as V_{GS}.

3. Explore the channel resistance / gate voltage relationship at low and high frequencies.

Questions to answer:

1. What is the gain function of your difference amplifier (if you used one)?

2. How do you find the channel resistance from the voltage over the drain resistor $(V_{DD} - V_D)$ and the values of the components used in the circuit?

3. Graph and discuss the $R_{ch}(V_{GS})$ curve.

13.3 Common-Source Amplifier

Instructions:

1. Using the 2n5459 n-channel JFET and the components below, build the Common Source Amplifier.

C_G	R_G	R_D	R_S	C_S	$\|V_{in}\|$
56 pF	10 MΩ	5100 Ω	1100 Ω	0.27 μF	60mV_{pp}

Table 13.1:

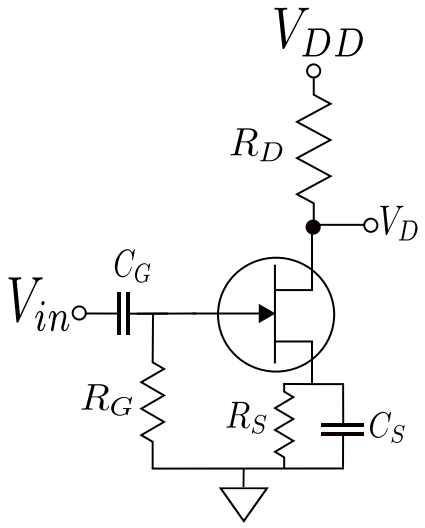

Figure 13.3: A common-source pnp JFET amplifier.

2. Measure the transmission A as a function of frequency.
3. The gain is probably much lower than we expect for an amplifier. Very R_S and R_D to get optimum gain.
4. Measure the transmission with this new configuration.

Questions to answer:

1. Plot the gain of the original configuration?
2. Why would R_S and R_D affect the gain? Explain using equations.
3. How much were you able to improve you gain?